
Variation Aware Adaptive Voltage Scaling For Digital Cmos Circuits

variation-aware adaptive tuning for nanophotonic interconnects - variation-aware adaptive tuning for nanophotonic interconnects rui wu1,; chin-hui chen 2, cheng li , tsung-ching huang , fan lan3, chong zhang1, yun pan4, john e. bowers 1, raymond g. beausoleil2, and kwang-ting cheng 1department of electrical & computer engineering, university of california, santa barbara, ca, us 2hp labs, hewlett-packard company, palo alto, ca, us **adaptive second-order total variation: an approach aware ...** - adaptive second-order total variation: an approach aware of slope discontinuities frank lenzen 1, florian becker , and jan lellmann2 1 heidelberg collaboratory for image processing (hci), heidelberg, germany 2 damtp, university of cambridge, uk abstract. total variation (tv) regularization, originally introduced by **varsha: variation and reliability-aware application ...** - varsha: variation and reliability-aware application scheduling with adaptive parallelism in the dark-silicon era nishit kapadia, sudeep pasricha department of electrical and computer engineering colorado state university, fort collins, co, u.s.a. nkapadia@colostate, sudeep@colostate abstract - with deeper technology scaling accompanied by a **variation-aware and adaptive timing optimisation methods ...** - variation-aware and adaptive timing optimisation methods in field programmable gate arrays zhenyu guan submitted in part fulfillment of the requirements for the degree of doctor of philosophy in electrical and electronic engineering of imperial college london. **variation aware adaptive voltage scaling for digital cmos ...** - [pdf]free variation aware adaptive voltage scaling for digital cmos circuits download book variation aware adaptive voltage scaling for digital cmos circuits.pdf (pdf) 32 bit×32 bit multiprecision razor-based dynamic ... fri, 29 mar 2019 04:08:00 gmt ieee transactions on very large scale integration (vlsi) systems, vol. 22, no. 4, april 2014 ... **adaptive temperature-aware soc test scheduling considering ...** - adaptive temperature-aware soc test scheduling considering process variation nima aghaee, zebo peng, and petru eles embedded systems laboratory (eslab), linkoping university, sweden {nimahaee, zebong, petru.eles}@liu abstract—high temperature and process variation are undesirable effects for modern systems-on-chip. the high **process variation aware dram (dynamic random access memory ...** - process variation aware dram (dynamic random access memory) design using block-based adaptive body biasing algorithm satyajit desai utah state university follow this and additional works at:<https://digitalcommons.usu.edu/etd> part of the computer engineering commons this thesis is brought to you for free and open access by the graduate **variation-aware application scheduling and power ...** - examine process variation in a cmp and point out the core-to-core variation in frequency. they estimate the maximum difference in core frequencies to be approximately 20%. they suggest adaptive body bias (abb) and adaptive supply voltage (asv) to reduce some of this variation — at the cost of increasing power variation. **560 ieee transactions on very large scale integration ...** - variation-aware adaptive voltage scaling system mohamed elgebaly, member, ieee, and manoj sachdev, senior member, ieee abstract—conventional voltage scaling systems require a delay margin to maintain a certain level of robustness across all possible device and wire process variations and temperature fluctuations. **vortex: variation-aware training for memristor x-bar** - robust variation-aware off-device training scheme, namely, vor-tex: vortex first modifies the programming pre-calculation algorithm to compensate the impact of memristor variations. it then introduces an adaptive mapping process that can selectively map the synapses having large impacts on network output onto the memristors with small variations. **a variation-aware design methodology for distributed ...** - 3. proposed variation-aware da computation the above observations show us that the da circuit consumes various clock cycles to generate the result bit in order and the corresponding critical path in each cycle has a very small delay difference. based on this characteristic, we propose to trade a small amount of area overheads to increase the **ieee transactions on computers, vol. 58, no. 7, july 2009 ...** - process variation-aware adaptive cache architecture and management madhu mutyam, member, ieee, feng wang, student member, ieee, ... process-variation-prone memory structures such as tlbs and l2 caches. for larger sized caches such as l2 caches, we can adopt our techniques by partitioning the cache into **a case for an adaptive and opportunistic variability ...** - a case for an adaptive and opportunistic variability-aware memory virtualization layer 39:3 2. motivation although there are many types of variability across different components, in this paper we will focus on memory variability, primarily two types: 1) off-the-shelf mem- **process-variation and soft-error reliability-aware ...** - variation-map data for a chip is available at run-time, in terms of the v t distribution, from the chip-frequency-profile obtained using ring-oscillator based delay sensors [12]; problem objective: given the above inputs and assumptions, our objective is to perform run-time application-scheduling and **design-time optimization of post-silicon tuned circuits ...** - design-time optimization of post-silicon tuned circuits using adaptive body bias sarvesh h. kulkarni, dennis m. sylvester, senior member, ieee, and david t. blaauw abstract—adaptive body biasing is a powerful technique that allows post-silicon tuning of individual manufactured dies such that each die optimally meets the delay and power ...

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